WHAT IS CLAIMED IS:

1. A silicon carbide n channel MOS semiconductor device, comprising:

a semiconductor substrate comprising silicon carbide, said substrate including a p base region, an n^+ source region and an n^+ drain region;

a gate insulating film formed on a surface of the p base region;

a gate electrode provided on the gate insulating film; and

first and second main electrodes that allow current to flow therebetween;

wherein current flowing between the first and second main electrodes is controlled by controlling an electron concentration of an inversion layer that is induced in a surface layer of the p base region located under the gate insulating film when a positive voltage is applied to the gate electrode; and

wherein an effective acceptor concentration measured in the vicinity of an interface between the p base region and the gate insulating film is in a range of 1×10^{13} to 1×10^{16} cm^{-3}.

2. A silicon carbide n channel MOS semiconductor device according to claim 1, wherein an impurity concentration of an inner part of the semiconductor substrate is higher than that in the vicinity of the interface between the p base region of the substrate and the gate insulating film.

3. A silicon carbide n channel MOS semiconductor device comprising:

a semiconductor substrate comprising silicon carbide, said substrate including a p base region, an n^+ source region and an n^+ drain region;

a gate insulating film formed on a surface of the p base region;

a gate electrode provided on the gate insulating film; and

first and second main electrodes that allow current to flow therebetween;

wherein current flowing between the first and second main electrodes is controlled by controlling an electron concentration of an inversion layer that is induced in a surface layer of the p base region located under the gate insulating film when a positive voltage is applied to the gate electrode; and

wherein a total amount x per unit area of donor impurities introduced into a surface layer of the p base region is in a range represented by:

$1 \times 10^{11}\ cm^{-2} < x < 5Q_B/q$,

$Q_B = (4\ \varepsilon o\ \varepsilon s\ \Phi_B\ N_A)^{1/2}$

where εo is a dielectric constant in vacuum, εs is a dielectric constant of silicon carbide, Φ_B is an energy difference between an intrinsic Fermi level and a Fermi level of silicon carbide, N_A is an acceptor concentration of the p base region before implantation of donor ions, and q is an intrinsic charge.

4. A silicon carbide n channel MOS semiconductor device according to claim 3, wherein the donor impurities introduced into the surface layer of the p base region comprise nitrogen or phosphorous.

5. A method for manufacturing a silicon carbide n channel MOS semiconductor device, comprising the steps of:

preparing a silicon carbide substrate comprising a p base region, an n^+ source region and an n^+ drain region;

forming a gate insulating film on a surface of the p base region;

forming a gate electrode on the gate insulating film; and

forming first and second main electrodes on the silicon carbide substrate such that current is allowed to flow between the first and second main electrodes;

wherein an effective acceptor concentration in the vicinity of an interface between the p base region and the gate insulating film is controlled to be in a range of 1×10^{13} to 1×10^{16} cm^{-3};

wherein current flowing between the first and second main electrodes is controlled by controlling an electron concentration of an inversion layer that is induced in a surface layer of the p base region located under the gate insulating film when a positive voltage is applied to the gate electrode; and

wherein the p base region is formed by ion implantation in which acceleration voltage and dose amount are controlled so that the acceptor concentration in the vicinity of the interface between the p base region and the gate insulating film is made lower than that in an inner part of the p base region.

6. A method for manufacturing a silicon carbide n-channel MOS semiconductor device, comprising the steps of:

preparing a silicon carbide substrate comprising a p base region, an n^+ source region and an n^+ drain region;

forming a gate insulating film on a surface of the p base region;

forming a gate electrode on the gate insulating film; and

forming first and second main electrodes on the silicon carbide substrate such that current is allowed to flow between the first and second main electrodes;

wherein an effective acceptor concentration in the vicinity of an interface between the p base region and the gate insulating film is controlled to be in a range of 1×10^{13} to 1×10^{16} cm^{-3};

wherein current flowing between the first and second main electrodes is controlled by controlling an electron concentration of an inversion layer that is induced in a surface layer of the p base region located under the gate insulating film when a positive voltage is applied to the gate electrode; and

wherein ions of donor impurities are implanted into the surface layer of the p base region in an amount that does not form an n-type region that is not depleted with zero bias, so that the effective acceptor concentration in the vicinity of the interface between the p base region and the gate insulating film is made lower than that in an inner part of the p base region.

7. A method according to claim 6, wherein the ions of donor impurities are implanted into the surface layer of the p base region in a dose amount "x" that is in a range represented by:

$1 \times 10^{11}\ cm^{-2} < x < 5Q_B/q$,

$Q_B = (4\ \varepsilon o\ \varepsilon s\ \Phi_B\ N_A)^{1/2}$

where εo is a dielectric constant in vacuum, εs is a dielectric constant of silicon carbide, Φ_B is an energy difference between an intrinsic Fermi level and a Fermi level of silicon carbide, N_A is an acceptor concentration of the p base region before implantation of donor ions, and q is an intrinsic charge.

8. A method according to claim 6 or 7, wherein the donor impurities comprise nitrogen or phosphorous.

9. A method according to any one of claims 5 through 7, further comprising a step of conducting heat treatment for activating impurities introduced by ion implantation.

10. A method according to claim 9, wherein the heat treatment is carried out at a temperature of 1000 to 1500°C.

11. A method for manufacturing a silicon carbide n-channel MOS semiconductor device, comprising the steps of:

preparing a silicon carbide substrate comprising a p base region, an n^+ source region and an n^+ drain region;

forming a gate insulating film on a surface of the p base region;

forming a gate electrode on the gate insulating film; and

forming first and second main electrodes on the silicon carbide substrate such that current is allowed to flow between the first and second main electrodes;

wherein an effective acceptor concentration in the vicinity of an interface between the p base region and the gate insulating film is controlled to be in a range of 1×10^{13} to 1×10^{16} cm^{-3};

wherein current flowing between the first and second main electrodes is controlled by controlling an electron concentration of an inversion layer that is induced in a surface layer of the p base region located under the gate insulating film when a positive voltage is applied to the gate electrode; and

wherein the surface layer of the p base region is formed by epitaxial growth so that the effective acceptor concentration in the vicinity of the interface between the p base region and the gate insulating film is made lower than that in an inner part of the p base region.